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| 10/594,040 | 09/25/2006 | Hideyuki Wada | Q96670 | 8971 |

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| MUNOZ, ANDRES F | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/594,040 | WADA ET AL. | |
| | Examiner | Art Unit | |
| | Andres Munoz | 2894 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 10-17* is/are pending in the application.

4a) Of the above claim(s) *7,8 and 10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20100413*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I (claims 1-6 and 14-17) in the reply filed on 09/13/2010 is acknowledged.

### *Claim Objections*

2. **Claim 1-6 and 14-17** are objected to because of the following informalities: where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p). Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 2, 5, 14 and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by Takao (US 2004/0137701 A1).

**Re claim 1**, Takao discloses a through wiring board provided with a through wiring (Fig. 8B) in a through hole (17) which is formed through a board (10), said through wiring board comprising:

the through hole (17) opened through said board (10) (Fig. 4, [0057], under broadest reasonable interpretation, hole 17 extends fully through layer 10, therefore meets the limitations as claimed);

a through extension wiring (20/21) with which said through hole is completely filled (20 completely fills 17) and which is formed on one surface of said through wiring board (bottom of Fig. 5) to extend (as 21) to a position at a predetermined distance from said through hole (Fig. 5, [0059-0062],"form…20 and…21 simultaneously"); and

a bump (23) having a conductivity, formed on said through extension wiring (20/21) and located in a position (overlying 16 in this case) other than the position where said through hole is opened (Fig. 8B, [0065]).

**Re claim 2**, Takao discloses an insulating layer (30) is provided between said board (10) and at least said through wiring and said through extension wiring (20/21) (Fig. 5, [0059]).

**Re claim 5**, Takao discloses a method of manufacturing a through wiring board provided with a through wiring (Fig. 8B) in a through hole (17) which is formed through a board (10), said method comprising:

a step of forming the through hole (17) opened through said board (10) (Fig. 4, [0057], under broadest reasonable interpretation, hole 17 extends fully through layer 10, therefore meets the limitations as claimed);

a step of forming a through extension wiring (20/21) on one surface (bottom of Fig. 5) of said through wiring board to completely fill (20 completely fills 17) said through hole and extend (as 21) to a position at a predetermined distance from said through hole (Fig. 5, [0059-0062],"form…20 and…21 simultaneously"); and,

a step of forming a bump (23) having a conductivity on said through extension wiring (20/21) in a position (overlying 16 in this case) other than the position where said through hole is opened (Fig. 8B, [0065]).

**Re claim 14**, Takao discloses a seed layer (18) disposed between the insulating (30) layer and the through extension wiring (20/21) (Fig. 5, [0060]).

**Re claim 16**, Takao discloses a step of forming an insulating layer (30) provided between said board (10) and at least said through wiring and said through extension wiring (20/21) (Fig. 5, [0059]); and

a step of forming a seed layer (18) disposed between the insulating layer (30) and the through extension wiring (20/21) (Fig. 5, [0060]).

5. **Claims 1, 4, 5 and 6** are rejected under 35 U.S.C. 102(e) as being anticipated by Imaoka (US 2004/0245649 A1).

6. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

**Re claim 1**, Imaoka discloses (Fig. 3) a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

the through hole (32) opened through said board (10/30/20) (Fig. 5B, [0078]);

a through extension wiring (38) with which said through hole is completely filled (with 40 & 42) and which is formed on one surface of said through wiring board to extend (as 40 & 42) to a position at a predetermined distance from said through hole (Fig. 6C, [0082-0083]); and

a bump (50) having a conductivity, formed on said through extension wiring (38) and located in a position other than the position where said through hole is opened (Fig. 3, [0085]).

**Re claim 4**, Imaoka discloses (Figs. 3) a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

the through hole (32) opened through said board (10/30/20) (Fig. 5B, [0078]);

an insulating resin layer (36) formed on (a portion of, as interpreted) the surface of said through wiring board except for the area where said through hole is opened in at least one surface of said through wiring board (Fig. 6A, [0080]);

a through extension wiring (38) with which said through hole is completely filled (with 40 & 42) and which is formed on said insulating resin layer (36) on said one surface of said through wiring board to extend (as 40 & 42) to a position at a predetermined distance from said through hole (Fig. 6C, [0082-0083]); and

a bump (50) having a conductivity, formed on said through extension wiring (38) and located in a position other than the position where said through hole is opened (Fig. 3, [0085]).

**Re claim 5**, Imaoka discloses (Fig. 3) a method of manufacturing a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

a step of forming the through hole (32) opened through said board (10/30/20) (Fig. 5B, [0078]);

a step of forming a through extension wiring (38) on one surface of said through wiring board to completely fill (with 40 & 42) said through hole and to extend (as 40 & 42) to a position at a predetermined distance from said through hole (Fig. 6C, [0082-0083]); and

a step of forming a bump (50) having a conductivity on said through extension wiring (38) in a position other than the position where said through hole is opened (Fig. 3, [0085]).

**Re claim 6**, Imaoka discloses (Figs. 3) a method of manufacturing a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

a step of forming the through hole (32) opened through said board (10/30/20) (Fig. 5B, [0078]);

a step of forming an insulating resin layer (36) on (a portion of, as interpreted) the surface of said through wiring board except for the area where said through hole is opened in at least one surface of said through wiring board (Fig. 6A, [0080]);

a step of forming a through extension wiring (38) on one surface of said insulating resin layer to completely fill (with 40 & 42) said through hole and extend (as 40 & 42) to a position at a predetermined distance from said through hole (Fig. 6C, [0082-0083]); and

a step of forming a bump (50) having a conductivity on said through extension wiring (38) in a position other than the position where said through hole is opened (Fig. 3, [0085]).

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 3, 4, 5 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanaoka et al. (of record, hereinafter "Hanaoka", US 2002/0030245 A1) in view of Lee et al. (US 6,844,627 B2).

**Re claim 1**, Hanaoka discloses a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

the through hole (4) opened through said board (6);

a through extension wiring (8) with which said through hole is filled (partially) and which is formed on one surface of said through wiring board (outside of hole 4 and towards element 20) to extend (as wire 18) to a position at a predetermined distance (towards element 20) from said through hole; and

a bump (24) having a conductivity, formed on said through extension wiring and located in a position (around element 20 as wire 18) other than the position where said through hole is opened (Fig. 1, [0122-0123]).

Hanaoka does not disclose a trough extension wiring with which said through hole is "completely" filled.

Lee discloses a trough extension wiring (38/40) with which said through hole (13) is completely filled (Fig. 2E, Col. 8 lines 45-55).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the completely filled hole of Lee to the device of Hanaoka so as to enable completely filled vias with conductive materials to thereby reduce contact/electrical resistances while avoiding formation of voids (Lee, Col. 1 lines 35-65 and Col. 8 lines 45-55. Moreover, Hanaoka addresses [0177] reduction of voids, while Lee addresses reduction of voids while fully filling a via with a conductive material, and as such, the examiner respectfully asserts the combination is proper).

**Re claim 3**, Hanaoka/Lee discloses (see Hanaoka) a through extension wiring (8) with which said through hole is filled in the other surface (opposite to surface where bump of claim 1 is disposed) of said through wiring board and which is formed on the

other surface of said through wiring board to extend (towards bump 80) to a position at a predetermined distance from said through hole; and a bump (80) having a conductivity, formed on said through extension wiring and located in a position other than the position where said through hole is opened (Fig. 13, [0200]. The examiner interprets the "other surface of…through wiring board" as that one opposite to the surface where first bump is formed).

**Re claim 4**, Hanaoka discloses a through wiring board provided with a through wiring in a through hole which is formed through a board, said through wiring board comprising:

the through hole (4) opened through said board (6);

an insulating resin layer (10) formed on the surface of said through wiring board (outside of hole 4 and towards element 20) except for the area where said through hole is opened in at least one surface of said through wiring board;

a through extension wiring (8) with which said through hole is filled (partially) and which is formed on said insulating resin layer on said one surface of said through wiring board to extend to a position at a predetermined distance (towards element 20) from said through hole; and

a bump (24) having a conductivity, formed on said through extension wiring and located in a position other than the position where said through hole is opened (Figs. 1, 7A, [0122-0123], [0144]).

Hanaoka does not disclose a trough extension wiring with which said through hole is "completely" filled.

Lee discloses a trough extension wiring (38/40) with which said through hole (13) is completely filled (Fig. 2E, Col. 8 lines 45-55).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the completely filled hole of Lee to the device of Hanaoka so as to enable completely filled vias with conductive materials to thereby reduce contact/electrical resistances while avoiding formation of voids (Lee, Col. 1 lines 35-65 and Col. 8 lines 45-55. Moreover, Hanaoka addresses [0177] reduction of voids, while Lee addresses reduction of voids while fully filling a via with a conductive material, and as such, the examiner respectfully asserts the combination is proper).

**Re claim 5**, Hanaoka discloses a method of manufacturing a through wiring board provided with a through wiring in a through hole which is formed through a board, said method comprising:

a step of forming the through hole (4) opened through said board (6);

a step of forming a through extension wiring (8) on one surface of said through wiring board to fill (partially) said through hole and extend to a position at a predetermined distance (towards element 20) from said through hole, and

a step of forming a bump (24) having a conductivity on said through extension wiring in a position other than the position where said through hole is opened (Figs. 1, 7A, 9C & 10C, [0122-0123], [0147], [0158], [0173]).

Hanaoka does not disclose a step of forming a through extension wiring on one surface of said through wiring board to “completely” fill said through hole.

Lee discloses a step of forming a through extension wiring (38/40) on one surface of said through wiring board to completely fill said through hole (13) (Fig. 2E, Col. 8 lines 45-55).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the completely filled hole of Lee to the method of Hanaoka so as to enable completely filled vias with conductive materials to thereby reduce contact/electrical resistances while avoiding formation of voids (Lee, Col. 1 lines 35-65 and Col. 8 lines 45-55. Moreover, Hanaoka addresses [0177] reduction of voids, while Lee addresses reduction of voids while fully filling a via with a conductive material, and as such, the examiner respectfully asserts the combination is proper).

**Re claim 6**, Hanaoka discloses a method of manufacturing a through wiring board provided with a through wiring in a through hole which is formed through a board, said method comprising:

a step of forming the through hole (4) opened through said board (6);

a step of forming an insulating resin layer (10) on the surface of said through wiring board (outside of hole 4 and towards element 20) except for the area where said through hole is opened in at least one surface of said through wiring board;

a step of forming a through extension wiring (8) on one surface of said insulating resin layer to fill (partially) said through hole and extend to a position at a predetermined distance (towards element 20) from said through hole; and

a step of forming a bump (24) having a conductivity on said through extension wiring in a position other than the position where said through hole is opened (Figs. 1, 7A, 9C & 10C, [0122-0123], [0144], [0147], [0158], [0173]).

Hanaoka does not disclose a step of forming a through extension wiring (8) on one surface of said insulating resin layer to completely fill said through hole.

Lee discloses a step of forming a through extension wiring (38/40) on one surface of said insulating resin layer (per Hanaoka) to completely fill said through hole (13) (Fig. 2E, Col. 8 lines 45-55).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the completely filled hole of Lee to the method of Hanaoka so as to enable completely filled vias with conductive materials to thereby reduce contact/electrical resistances while avoiding formation of voids (Lee, Col. 1 lines 35-65 and Col. 8 lines 45-55. Moreover, Hanaoka addresses [0177] reduction of voids, while Lee addresses reduction of voids while fully filling a via with a conductive material, and as such, the examiner respectfully asserts the combination is proper).

9. **Claims 4, 6, 15 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao in view of Hanaoka et al. (of record, hereinafter "Hanaoka", US 2002/0030245 A1).

**Re claim 4**, Takao discloses a through wiring board provided with a through wiring (Fig. 8B) in a through hole (17) which is formed through a board (10), said through wiring board comprising:

the through hole (17) opened through said board (10) (Fig. 4, [0057], under broadest reasonable interpretation, hole 17 extends fully through layer 10, therefore meets the limitations as claimed);

a through extension wiring (20/21) with which said through hole is completely filled (20 completely fills 17) and which is formed on *one surface of said through wiring board* (bottom of Fig. 5) to extend (as 21) to a position at a predetermined distance from said through hole (Fig. 5, [0059-0062],"form…20 and…21 simultaneously"); and

a bump (23) having a conductivity, formed on said through extension wiring (20/21) and located in a position (overlying 16 in this case) other than the position where said through hole is opened (Fig. 8B, [0065]).

Takao does not disclose:

- An insulating resin layer formed on the surface of said through wiring board except for the area where said through hole is opened in at least one surface of said through wiring board, and,

- A through extension wiring with which said through hole is completely filled and which is formed on "*said insulating resin layer on said one surface of said thru wiring board".*

Hanaoka discloses:

- An insulating resin layer (10) formed on the surface of said through wiring board (6) except for the area (52) where said through hole (4) is opened in at least one surface of said through wiring board (Fig. 7B, [0123], [0149-0152]).

- A through extension wiring (8/18) with which said through hole is completely filled (per Takao) and which is formed on "*said insulating resin layer on said one surface of said thru wiring board"* (Figs. 7B & 10A, [0123], [0149-0152], [0165]. Including layer 10 of Hanaoka in the device of Takao implicitly meets the limitations as claimed, since as understood, said layer 10 of Hanaoka is included in Takao prior to defining the through extension wiring).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include insulating resin of Hanaoka to the device of Takao so as to improve electrical insulation between a conductive materials and IC devices (Hanaoka, [0123]).

**Re claim 6**, Takao discloses a method of manufacturing a through wiring board provided with a through wiring (Fig. 8B) in a through hole (17) which is formed through a board (10), said method comprising:

a step of forming the through hole (17) opened through said board (10) (Fig. 4, [0057], under broadest reasonable interpretation, hole 17 extends fully through layer 10, therefore meets the limitations as claimed);

a step of forming a through extension wiring (20/21) on *one surface of said through wiring board* (bottom of Fig. 5) to completely fill (20 fills 17) said through hole and extend (as 21) to a position at a predetermined distance from said through hole (Fig. 5, [0059-0062],"form…20 and…21 simultaneously"); and

a step of forming a bump (23) having a conductivity on said through extension wiring (20/21) in a position (overlying 16 in this case) other than the position where said through hole is opened (Fig. 8B, [0065]).

Takao does not disclose:

- A step of forming an insulating resin layer on the surface of said through wiring board except for the area where said through hole is opened in at least one surface of said through wiring board; and,

- A step of forming said through extension wiring on "*one surface of said insulating resin*" to completely fill said through hole.

Hanaoka discloses:

- A step of forming an insulating resin layer (10) on the surface of said through wiring board (6) except for the area (52) where said through hole (4) is opened in at least one surface of said through wiring board (Fig. 7B, [0123], [0149-0152]); and,

- A step of forming said through extension wiring (8/18) on "*one surface of said insulation resin (10)* to completely fill (per Takao) said through hole (Figs. 7B & 10A, [0123], [0149-0152], [0165]. Including layer 10 of Hanaoka in the device of Takao implicitly meets the limitations as claimed, since as understood, said layer 10 of Hanaoka is included in Takao prior to defining the thru extension wiring).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include insulating resin of Hanaoka to the method of Takao so as to improve electrical insulation between a conductive via materials and IC devices (Hanaoka, [0123]).

**Re claim 15**, Takao/Hanaoka discloses (see Takao) an insulating layer (30) is provided between said board (10) and at least said through wiring and said through extension wiring (20/21) (Fig. 5, [0059]); and

a seed layer (18) disposed between the insulating layer (30) and the through extension wiring (20/21) (Fig. 5, [0060]).

**Re claim 17**, Takao/Hanaoka discloses (see Takao) a step of forming an insulating layer (30) is provided between said board (10) and at least said through wiring and said through extension wiring (20/21) (Fig. 5, [0059]); and

a step of forming a seed layer (18) disposed between the insulating layer (30) and the through extension wiring (20/21) (Fig. 5, [0060]).

## *Response to Arguments*

10. Applicant's arguments with respect to claims 1-6 and 14-17 have been considered but are moot in view of the new ground(s) of rejection. Argument(s) based on the newly added limitation(s) is/are addressed in the above rejection.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andres Munoz whose telephone number is (571) 270-3346. The examiner can normally be reached on 7:30am - 4:00pm (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andres Munoz/
Examiner, Art Unit 2894
September 20, 2010

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894